

DESIGN OF LOW POWER TEST PATTERN GENERATOR

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ABSTRACT

Test pattern generator is more suitable for built in self test (BIST) structures used for testing of VLSI circuits. The objective of BIST is to reduce power dissipation. The main aim of the project is to design and implement design of low power test pattern generator (TPG) using LP-LFSR. LFSR and counter are designed with 14 transistor's D flip flop. This increases more power consumption and delay. Area occupied by the circuit is also large. The proposed test pattern generator reduces power consumption and delay. In this approach LFSR and counter are designed with 5 transistor D flip flop which reduces power consumption and delay. The proposed method is faster when compared to area and speed.

KEYWORDS: BIST, D Flip Flop, LFSR, Test Pattern Generator